CLAIM AMENDMENTS

1. (Original) An apparatus for supplying current to a semiconductor device during a test of the semiconductor device by an integrated circuit tester accessing input/output (I/O) terminals of the semiconductor device via interface means providing signal paths between the I/O terminals and the integrated circuit tester, wherein the semiconductor device includes a power input terminal for receiving supply current via a power conductor provided by the interface means, and wherein the semiconductor device temporarily increases its demand for supply current following each of a set of edges of a clock signal applied as input to the semiconductor device, the apparatus comprising:

first means for supplying a first current to the power input terminal during the test;

second means for supplying a current pulse to the power input terminal following each of the edges of the clock signal supplementing the first current, wherein a magnitude of the current pulse is a function of magnitudes represented by a prediction signal and an adaption signal; and

third means for adjusting the magnitude represented by the adaption signal in response to a voltage appearing at the power input terminal,

wherein the magnitude represented by the prediction signal is set proportional to a predicted amount by which the semiconductor device will increase its demand for current at its power input terminal following a next one of the clock signal edges.

2-24 (Canceled)